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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/696,716	MORITA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *65-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *65-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/28/03;2/21/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 65-77 are pending in the Application.

Claims 75-77 are new.

Claims 1-64 are cancelled.

Claims 66, 67 and 73 are amended.

Claims 65-77 are rejected.

Response to Amendment

2. Applicant's amendments and arguments filed on 24 May 2007 in response to the office action mailed on 10 August 2006 have been fully considered, but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 28 October 2003 and 21 February 2007 were fully considered by the examiner.

Claim Objections

4. Claim 69 is objected to because of the following informalities:

The phrase "mode register is indicated access mode" should be changed to "mode register indicates an access mode" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 65-72 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

As for claim 65, a process is set forth, defined by a step of "detecting a write operation", which alone fails to sufficiently create a "useful, concrete and tangible result". It is worthy to note that claim 65 does in fact recite a *conditional* tangible result (i.e. writing to non-volatile memory), however this result is contingent upon determining if the write operation is directed to a first or second memory area. Since the claims fail to *ensure* a "useful, concrete and tangible result" from the recited steps (i.e. if neither of the if statements are true, the only remaining limitation is memory access detection step), they are held to be non-statutory. A similar rejection applies to claim 67 for only reciting only a similar detecting step and determining step, without ensuring a "useful, concrete and tangible result".

Claims 66 and 68-72 are rejected for further inheriting the deficiencies of claims 65 and 67.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 65-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner notes that there are so many issues in these claims, that use of the formal paragraphs would be inefficient. Examiner will now address, claim by claim, the issues which render the instant claims vague and indefinite.

As for claim 65, the phrase "address of said write operation" as recited in lines 4 and 7 render the claim indefinite. Is the address of the write operation the address of command itself, or the address to which said operation is directed to write? A similar rejection applies to claim 73, lines 5 and 7; and claim 76, lines 6 and 8. Additionally, the phrase "the first write operation speed" as recited in lines 9-10 lacks antecedent basis as "a first write operation speed" is not previously set forth in the claim. A similar rejection applies to claim 73, line 11 for "the second write operation speed".

As for claim 66, the phrase "said first write operation is a fast write operation which is a shorter time than a predetermined time to write said non-volatile memory" renders the claim indefinite. How can a write operation be defined by a period of time? Does this recitation refer to the time in which said fast write operation takes to execute? A similar rejection applies to claim 77, lines 1-2. Additionally, the phrase "a slow operation which is executed in accordance with the predetermined time" renders the claim indefinite. What exactly constitutes executing "in accordance" to a predetermined time? For examples, does this said slow write operation execute within said

predetermined time, or is it delayed by said predetermined time? A similar rejection applies to claim 77, line 4.

As for claim 67, the phrase "determining an access mode of said non-volatile memory corresponding to a mode register" renders the claim indefinite. What exactly constitutes an access mode as "corresponding" to a mode register? Does the mode register store information indicative of the access mode of said memory? Additionally, the phrase "if an address of said non-volatile memory from a processing logic is indicated to a [first and second] address area" as recited in lines 8-9 and 11-12 renders the claim indefinite. More specifically, how exactly can an address be "indicated to" an first or second address area? Does this recitation refer to an address *addressing a location* located within a first or second memory area?

As for claim 68, the phrase "cache memory stores other data in said cache write operation of said data" renders the claim indefinite. How can "other data" be stored "in [a] cache write operation"?

As for claim 71, the phrase "said first address area and said second address area is indicated in a register" renders the claim indefinite. What exactly constitutes an address area as being "indicated in a register"? Does said register store the address information (i.e. start/end locations of the area), or the status (i.e. free, occupied, etc?) of each of the respective memory areas?

As for claim 72, the phrase "detecting a write operation to the re-programmable non-volatile memory is based on identifying the write operation" renders the claim indefinite. How exactly can "detecting a write operation" be "based on identifying a write

operation"? Is the detection contingent upon the type of write operation, or which address (i.e. first or second area) in which the operation is directed? Additionally, "the write operation" as recited in line 3 of the claim lacks antecedent basis as both a first and second write operation are previously set forth in claim 65. Which operation is being referred to here? A similar rejection applies to claim 74, line 3.

Claims 69, 70 and 75 are rejected for further inheriting the deficiencies of claim 67, 68 and 73 respectively.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 65, 66 and 72-77 are rejected under 35 U.S.C. 102(b) as being anticipated by Tobita et al. (US PG Publication 2002/0051394 A1), hereinafter Tobita.

As for claim 65, Tobita teaches a memory access method comprising:

detecting a write operation to a memory including a re-programmable non-volatile memory (Fig. 48, elements 1239 and 1014 comprise the memory which is a mix of slow write and fast write memory banks (see also paragraph 0240, all lines) - paragraph 0047, all lines – data is initially stored in a write buffer. Once the transfer from the host terminates, the data is written to the flash memory (i.e.

non-volatile memory). The system must inherently detect a write operation before a write can be performed);

if an address of said write operation from a processor logic indicates a first address area of said non-volatile memory, then performing a first write operation of data to said non-volatile memory (Fig. 48 – element 1014 – at least the high order bits are written via a fast write operation); and

if said address of said write operation from a processor logic indicates a second address area of said non-volatile memory, then performing a second write operation of data to said non-volatile memory according to a write operation speed that is different from the first write operation speed (Fig. 48 – element 1239 – the low order bits (for example) are written via a slow write operation).

As for claim 73 Tobita teaches a data processing unit comprising:

memory, including a re-programmable non-volatile memory (Fig. 48, elements 1239 and 1014 comprise the memory which is a mix of slow write and fast write memory banks (see also paragraph 0240, all lines)); and

control logic (the card controller (Fig. 48) and the control microcomputer (Fig. 1 – element 1007) work in conjunction to control memory access (i.e. bank and address)) configured for detecting a write operation to the memory and for performing said write operation according to an operation mode in which the control logic determines if an address of said write operation from a processor logic indicates a first address area of said non-volatile memory and performs a first write operation of data to said non-volatile memory, and if said address of

said write operation from a processor logic indicates a second address area of said non-volatile memory, then performs a second write operation of data to said non-volatile memory (Fig. 48 – element 1014 – at least the high order bits are written via a fast write operation and the lower order bits of Fig. 48 element 1239 are written via a slow write operation);

wherein the first write operation is performed at a write operation speed that is different from the second write operation speed (the slow access time flash and fast access time flash banks are accessed at different speeds).

As for claim 76, Tobita teaches a data processing unit comprising:

memory that includes re-programmable non-volatile memory into which data is written (Fig. 48, elements 1239 and 1014 comprise the memory which is a mix of slow write and fast write memory banks (see also paragraph 0240, all lines)); and

control logic (the card controller (Fig. 48) and the control microcomputer (Fig. 1 – element 1007) work in conjunction to control memory access (i.e. bank and address)) configured for detecting a write operation to the memory and for performing the write operation to a first address area of the non-volatile memory at a first write operation speed if an address of the write operation indicates a first memory area of the memory and for performing the write operation to a second address area of the non-volatile memory at a second write operation speed if an address of the write operation indicates a second memory area of the memory, wherein the first write operation speed is different from the second write

operation speed (Fig. 48 – element 1014 – at least the high order bits are written via a fast write operation and the lower order bits of Fig. 48 element 1239 are written via a slow write operation. Note, by their very definition, the slow access time flash and fast access time flash banks are accessed at slow and fast speeds respectively).

As for claim 66, Tobita teaches said first write operation is a fast write operation which is a shorter time than a predetermined time to write said non-volatile memory (by definition, the fast write flash has a faster access time than the slow flash); and

wherein said second write operation is a slow write operation which is executed in accordance with the predetermined time to write said non-volatile memory (the predetermined time is equal to the duration to execute a slow write operation).

As for claim 72, Tobita teaches detecting a write operation to the re-programmable non-volatile memory is based on identifying the write operation as directed to a predetermined address space that corresponds to the re-programmable non-volatile memory (the system must inherently determine which address (and which memory bank (i.e. Fig. 48, elements 1239 and 1014)) it is writing the data to before its written. Data written to the former bank is written with slow access time, and the latter is written with a fast access time).

As for claim 74, Tobita teaches the control logic detects a write operation to the re-programmable non-volatile memory by identifying the write operation as directed to a predetermined address space that corresponds to the re-programmable non-volatile

memory (the system must inherently determine which address (and which memory bank (i.e. Fig. 48, elements 1239 and 1014)) it is writing the data to before its written. Data written to the former bank is written with slow access time, and the latter is written with a fast access time).

As for claim 75, Tobita teaches the first write operation is a fast write operation and the second write operation is a slow write operation (by their very definition, fast flash and slow flash are written via fast and slow writes respectively).

As for claim 77, Tobita teaches said first write operation is a fast write operation that is a shorter time than a predetermined time to write said non-volatile memory; and wherein said second write operation is a slow write operation which is executed in accordance with the predetermined time to write said non-volatile memory (by definition, the fast write flash has a faster access time than the slow flash. The predetermined time is equal to the duration to execute a slow write operation).

8. Claims 67-71 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. (US Patent 4,969,121), hereinafter Chan.

As for claim 67, Chan teaches a memory access method comprising:

detecting a write operation to a non-volatile memory (Chan teaches controlling the speed (either via slow speed or fast speed) of access operations to a non-volatile (i.e. EPROM) array – col. 1, line 47 through col. 2, line 6 and col. 2, lines 47-58. Since Chan's system writes to a non-volatile array, it must inherently detect a write operation for it to occur);

determining an access mode of said non-volatile memory corresponding to a mode register for controlling said non-volatile memory, if said access mode is a first mode, then performing a fast write operation of data to said non-volatile memory (col. 7, lines 47-67 – either slow read/write mode or fast read/write mode is selected via the select elements 34 and 36 depicted in Fig. 4. If fast mode is selected (direct access control), the system will determine that fast mode access is required),

if said access mode is a second mode, then performing a slow write operation of data to said non-volatile memory (Referring to Fig. 4, element 36 (for example) contains the slow option bit to indicate slow access mode. If slow mode is selected, the system will determine that slow access (i.e. increased propagation) is required),

if said access mode is a third mode write operation (Chan's system only has fast and slow modes (not a combination of both), therefore in Chan's system the third "if statement" will never be true, hence his system is not required to function as recited when the recited "if statement" is true)

if said access mode is a fourth mode, (Chan's system only has fast and slow modes (not a fourth with caching functionality), therefore in Chan's system the fourth "if statement" will never be

true, hence his system is not required to function as recited when the "if statement" is true).

As for claim 68, Chan's system only has fast and slow modes (not a fourth with caching functionality), therefore in Chan's system the fourth "if statement" will never be true, hence his system is not required to function as recited when the "if statement" is true).

As for claim 69, Chan teaches said mode register is indicated access mode for said non-volatile memory (referring to Fig. 4, element 36 depicts the slow option bit to indicate slow access mode. If slow mode is selected, the system will determine that slow access (i.e. increased propagation) is required).

As for claim 70, Chan teaches said slow write operation has a predetermined write time to said non-volatile memory (the predetermined time equals the actual access time plus increased propagation); and

wherein said fast write operation has a write time shorter than said predetermined time of said slow write time (fast write access by its very definition is faster than the slow access mode).

As for claim 71, Chan teaches first and second modes only (slow or fast, but not a combination as recited by the third mode), hence he is not required to teach elements recited only when this particular "if statement" is true.

9. Claims 67-71 are rejected under 35 U.S.C. 102(b) as being anticipated by Naiki et al. (US Patent 6,075,723), hereinafter Naiki.

As for claim 67, Naiki teaches a memory access method comprising:

detecting a write operation to a non-volatile memory (Fig. 1, elements 11a-11d depict the non-volatile flash memory. Since Naiki's system writes to a non-volatile memory, it must inherently detect a write operation for it to occur;

determining an access mode of said non-volatile memory corresponding to a mode register for controlling said non-volatile memory, if said access mode is a first mode, then performing a fast write operation of data to said non-volatile memory (Fig. 11b depicts a memory for storing mode information. The mode can be long play (LP, i.e. slow write), or short play (SP, i.e. fast write), or a combination thereof –col. 5, lines 6-47). Fig. 2B, the entire memory is configured as LP.

if said access mode is a second mode, then performing a slow write operation of data to said non-volatile memory (Fig. 2A, the entire memory is configured as SP),

if said access mode is a third mode write operation (combination of LP and SP modes), then:

if an address of said non-volatile memory from a processing logic is indicated to a first address area, then said non-volatile memory write operation is executed according to said fast write operation of data (Fig. 3A depicts some addresses as SP and some as LP – col. 5, lines 6-47),

if an address of said non-volatile memory is indicated to a second address area, then said non-volatile memory

write operation is executed according to said slow write operation of data (Fig. 3A depicts some addresses as SP and some as LP – col. 5, lines 6-47); and

if said access mode is a fourth mode, (Naiki's system only has three modes: fast, slow and a combination thereof – not a fourth with caching functionality, therefore in Naiki's system the fourth "if statement" will never be true, hence his system is not required to function as recited when the "if statement" is true).

As for claim 68, Naiki's system only has three modes: fast, slow and a combination thereof – not a fourth with caching functionality, therefore in Naiki's system the fourth "if statement" will never be true, hence his system is not required to function as recited when the "if statement" is true.

As for claim 69, Naiki teaches said mode register is indicated access mode for said non-volatile memory (as discussed in claim 67, Fig. 11b depicts storing modes of the flash memory).

As for claim 70, Naiki teaches said slow write operation has a predetermined write time to said non-volatile memory and wherein said fast write operation has a write time shorter than said predetermined time of said slow write time (the SP mode is faster than the reduced write time of the LP mode).

As for claim 71, Naiki teaches said first address area and said second address area is indicated in a register (the address areas of the register illustrated in Fig. 3B indicate which areas are SP and which are LP).

Response to Arguments

10. Applicant's arguments (filed in the original response dated 21 February 2007 and the fully responsive response filed 24 May 2007) with respect to the comparison between the instant claims and Tobita, have been fully considered, however they are not persuasive.

Applicant asserts, "Tobita (US2002/0051394) describes a controller in Fig. 48 that connects three flash modules in which two modules are slow-access flash memory 1239 and one module is fast-access flash memory 1014. The writing speed, however, is fixed according to the flash memory module and therefore Tobita does not teach changing the access speed based on an operation mode (including fast access mode and slow access mode)."

This statement however is not persuasive as the argument is not commensurate with the scope of the instant claims. The independent claims (65 for example), require performing a first write operation on a first area of memory and a second write operation on a second area of memory, wherein the first and second write speeds are different. Tobita in fact anticipates these limitations with the three memory banks (two slow, one fast) as discussed in the Tobita 35 USC § 102(b) rejection, *supra*. The instant independent claims presently rejected by Tobita do not require "changing the access speed based on an operation mode", Applicant's arguments notwithstanding. It is worthy to note that claim 73 requires "an operation mode" in which a fast write or slow write is performed based on an *address*. Nowhere however, does this claim require

"changing the access speed based on an operation mode" as alleged by Applicant. Rather, the write speed is determined based on the location (i.e. address), which is clearly anticipated by Tobita as discussed in the claim rejections, *supra*.

Applicant's arguments with respect to Tobita failing to teach accessing a cache memory based on access mode is rendered moot in view of the new grounds of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
7/27/07